80 via a control port. SIGNAL is indicated by 2 control bits and then formatted as described. The interface **80** provides the LENGTH in μs. CRC in PLCP header is performed on SIGNAL, SERVICE and LENGTH fields.

MPDU is serially provided by Interface **80** and is the variable data scrambled for normal operation. The reference phase for the first symbol of the MPDU is the output phase of the last symbol of the header for Diff Encoding. The last symbol of the header into the scrambler **51** must be followed by the first bit of the MPDU. The variable data may be modulated and demodulated in different formats than the header portion to thereby increase the data rate, and while a switchover as indicated by the switchover point in FIG. **3**, occurs on-the-fly.

Turning now additionally to FIG. **4**, the timing of the high data rate modulator **50** may be further understood. With the illustrated timing, the delay from TX_RDY to the first Hi Rate Output Chip is ten 11 MHz clock periods or 909.1 ns. The other illustrated quantities will be readily appreciated in view of the above description.

Referring now to FIG. **5**, the high data rate demodulator **60** in accordance with the invention is further described. The high rate circuits are activated after the signal field indicates 5.5 or 11 Mbit/s operation. At a certain time, the start phase is jammed into the Carrier NCO **61** and the start frequency offset is jammed into the Carrier Loop Filter **62**. The signal is frequency translated by the C/S ROM **63** and the Complex Multiplier **64** and passed to the Walsh Correlator **65**. The correlator **65** output drives the Symbol Decision circuits **66**, as illustrated. The output of the Symbol Decision circuits **66** are serially shifted by the parallel-in/serial-out SIPO block **67** to the descrambler portion of the PSK Demodulator and Scrambler circuit **70** after passing through the Sign Correction circuit **68** based on the last symbol of the header. The timing of the switch over desirably makes the symbol decisions ready at the correct time.

The signal is phase and frequency tracked via the Complex Multiplier **64**, Carrier NCO **61** and Carrier Loop Filter **62**. The output of the Complex Multiplier **64** also feeds the Carrier Phase Error Detector **76**. A decision directed Chip Phase Error Detector **72** feeds the illustrated Timing Loop Filter **75** which, in turn, is connected to the Clock Enable Logic **77**. A decision from the Chip Phase Error Detector **72** is used instead of early-late correlations for chip tracking since the SNR is high. This greatly reduces the additional circuitry required for high rate operation. The 44 MHz master clock input to the Clock Control **74** will allow tracking high rate mode chips with ±⅛ chip steps. Only the stepper is required to run at 44 MHz, while most of the remaining circuits run at 11 MHz. The circuit is only required to operate with a long header and sync.

Turning now additionally to FIG. **6**, a pair of Walsh Correlators **65***a*, **65***b* is further described. The I_END and Q_END inputs from the chip tracking loop are input at 11 MHz. The Modified Walsh Generator **81** produces the 8 Walsh codes (W0 to W7) serially to sixteen parallel correlators (8 for I_END and 8 for Q_END). The sixteen correlations are available at a 1.375 MHz rate. The Walsh Codes (W0 to W7) are the same as listed in the table above for the high data rate modulator. For the 11 Mbit/s mode, the largest magnitude of I W0 to I W7 is selected by the Pick Largest Magnitude circuit **81***a* to form I sym. I sym is formatted in Sign-Magnitude. The Magnitude is the Modified Walsh Index (0 to 7) of the largest Correlation and Sign is the sign bit of the input of the winning Correlation. The Q channel is processed in parallel in the same manner. For the 5.5 Mbit/s mode, the largest magnitude of I W0 to I W7 is selected to form Isym. In this case, only I sym is output. AccEn controls the correlator timing and is supplied by timing and control circuits.

With additional reference to FIG. **7**, the carrier tracking loop **90** is now described. In the described embodiment, the number of bits are worst case for estimation purposes. While 3 bits are used for the A/D conversion, a higher number may be desired in other embodiments as would be readily appreciated by those skilled in the art. The Phase BIAS circuit **91** compensates for constellation rotation, that is, BPSK or QPSK. FSCALE compensates for the NCO clock frequency. PHASE SCALE compensates for a phase shift due to frequency offset over the time difference of the first and second loops. The Lead and Lag Shifters **92**, **93** form the loop multiplier for the second order carrier tracking loop filter **62**.

Referring now additionally to FIG. **8**, the Chip Tracking Loop **110** is further described. All circuits except Chip Advance/Retard **111** use the 22 MHz clock signal. The Chip Advance/Retard circuit **111** may be made to integrate with the existing clock of the prior art PRISM 1 circuit. PRISM 1 steps in ±¼ chips. The PRISM 1 timing may be changed to switchover this circuit for high data rate operation. The A/D clock switches without a phase shift. I_ROT and Q_ROT are from the Complex Multiplier **64** at 22 MHz. They are sampled by the illustrated Registers **112** to produce I_End and Q_End at 11 MHz, which are routed to the Correlators **65** (FIG. **6**). The alternate samples I_Mid and Q_Mid are used to measure the chip phase error. For QPSK, errors are generated from both rails, and for BPSK, the error is only generated from the I rail. QPSK En disables the Q rail phase error for BPSK operation.

The sign of the accumulator is used to advance or retard the chip timing by ⅛ chip. This circuit must be enabled by the PRISM 1 circuits at the proper time via the HI_START signal. The errors are summed and accumulated for 32 symbols (256 chips). The Chip Track Acc signal them dumps the accumulator for the next measurement. The chip phase error is generated if the End Sign bits bracketing the Mid sample are different. This is accomplished using the transition detectors. The sign of the chip phase error is determined by the sign of the End sample after the Mid sample. A multiplier **114** is shown for multiplying by +1 if the End Sign is 0 or by −1 if the End Sign is 1. If the End sign bits are identical, the chip phase error for that rail is 0. The AND function is only enabled by transitions.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

That which is claimed is:

1. A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit connected thereto, said baseband processor comprising

a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit,

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to said radio circuit,

said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code reducing

an average DC signal component which in combination with the AC-coupling to said at least one A/D converter enhances overall performance, and

a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

2. A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

3. A spread spectrum radio transceiver according to claim 2 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

4. A spread spectrum radio transceiver according to claim 3 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

5. A spread spectrum radio transceiver according to claim 3 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

6. A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

7. A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

8. A spread spectrum radio transceiver according to claim 1 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

9. A spread spectrum radio transceiver according to claim 1 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

10. A spread spectrum radio transceiver according to claim 1 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel connected correlators connected to said modified Walsh function generator.

11. A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

12. A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

13. A spread spectrum radio transceiver according to claim 1 wherein said demodulator comprises clear channel assessing means for generating a clear channel assessment signal.

14. A spread spectrum radio transceiver according to claim 1 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator connected to said baseband processor; and

an up/down frequency converter connected to said quadrature intermediate frequency modulator/demodulator.

15. A spread spectrum radio transceiver according to claim 14 wherein said radio circuit further comprises:

a low noise amplifier having an output connected to an input of said up/down converter; and

a radio frequency power amplifier having an input connected to an output of said up/down converter.

16. A spread spectrum radio transceiver according to claim 15 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

17. A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code reducing an average DC signal component to thereby increase AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one predetermined orthogonal code function encoder for encoding information according to the predetermined orthogonal code.

18. A baseband processor according to claim 17 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

19. A baseband processor according to claim 18 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

20. A baseband processor according to claim 19 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

21. A baseband processor according to claim 19 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

22. A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

23. A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

24. A baseband processor according to claim 17 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder.

25. A baseband processor according to claim 17 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

26. A baseband processor according to claim 17 wherein the predetermined orthogonal code is a bi-orthogonal code.

27. A baseband processor according to claim 17 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

28. A baseband processor according to claim 17 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

29. A baseband processor according to claim 17 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

30. A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

means for operating in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate,

header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising

at least one correlator for decoding received information,

means for operating in one of the first and second formats,

header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,

a first carrier tracking loop for the third format, and

a second carrier tracking loop for the first and second formats.

31. A baseband processor according to claim 30 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

32. A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

33. A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

34. A baseband processor according to claim 30 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

35. A baseband processor according to claim 30 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

36. A modulator for a spread spectrum radio transceiver, said modulator comprising:

modulator means for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator means comprising at least one predetermined orthogonal code function encoder for encoding information according to a predetermined orthogonal code for reducing an average DC signal component.

37. A modulator according to claim 36 wherein said modulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

38. A modulator according to claim 37 wherein said modulator means comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats.

39. A modulator according to claim 38 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

40. A modulator according to claim 36 wherein said modulator means further comprises means for partitioning

data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder, and wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

41. A modulator according to claim **36** wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

42. A modulator according to claim **36** wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

43. A modulator according to claim **36** wherein the predetermined orthogonal code is a bi-orthogonal code.

44. A demodulator for a spread spectrum radio transceiver, said demodulator comprising:

demodulator means for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit, said demodulator means comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code reducing an average DC signal component.

45. A demodulator according to claim **44** wherein said demodulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

46. A demodulator according to claim **45** wherein said demodulator means comprises header demodulator means for demodulating data packets including a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

47. A demodulator according to claim **46** wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

48. A demodulator according to claim **46** wherein said demodulator means further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

49. A demodulator according to claim **48** wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

50. A demodulator according to claim **48** wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

51. A demodulator according to claim **44** further comprising means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits).

52. A demodulator according to claim **44** wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

53. A demodulator according to claim **44** wherein the predetermined orthogonal code is a bi-orthogonal code.

54. A demodulator according to claim **44** wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

55. A method for baseband processor for spread spectrum radio communication, the method comprising the steps of:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to the predetermined orthogonal code for reducing an average DC signal component; and

spread spectrum PSK demodulating received information by decoding the received information according to the predetermined orthogonal code.

56. A method according to claim **55** further comprising the step of AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

57. A method according to claim **55** further comprising the steps of modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

58. A method according to claim **57** further comprising the steps of:

modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

59. A method according to claim **58** wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

60. A method according to claim **55** wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

61. A method according to claim **55** wherein the predetermined orthogonal code is a bi-orthogonal code.

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